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EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/672,437	NALBANT, MEHMET K.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,15-26,28 and 29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12, 15-26, 28 and 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2-4, 12, 15-18 and 28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 2, the recitation "controlled rate is a predetermined rate of voltage increase" is indefinite because it is not clear what is this rate and what is the "predetermined rate". Page 6 of the specification discloses a "slew rate" that is only a kind of delay. The same rationale is applied to claims 3-4, 15-18 and 28.

Regarding claim 12, the recitation " further comprising switching transistors in the integrated circuit, the switching transistors being coupled to an output of the pulse width modulation switching regulator controller circuit" is indefinite because it is not clear what are "switching transistors" in the drawing. Assume that the circuit of claim 12 reads in figure 2; figure 2 does not show these switching transistors". The recitation "the integrated circuit" lacks antecedent basis.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 7-11, 15-18, 21-25, 28 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Patel et al. US (Pat. 6,456,510).

Regarding claim 1, figures 7 and 10 of Patel show a hot swappable pulse width modulation switching regulator controller comprising:

a hot swap transistor (Q1);

a pulse width modulation switching regulator controller circuit (PWM COMP) coupled in series with the hot swap transistor;

a hot swap circuit (901) coupled to a control terminal of the hot swap transistor;

the hot swap circuit, when the hot swap circuit and the series combination of the hot swap transistor and the pulse width modulation switching regulator controller circuit are coupled to an active source of power (Vin), turning on the hot swap transistor (901) at a controlled rate;

whereby power is applied to the pulse width modulation switching regulator controller circuit at a controlled rate in spite of the sudden application of power to the hot swappable pulse width modulation switching regulator controller (col. 12, lines 13-48);

the pulse width modulation switching regulator controller circuit and the hot swap circuit inherently being in a single integrated circuit.

Regarding claims 2, 3 and 4, because of the (PWM), control circuit (902) and the transformer (T2), the control voltage applied to the gate of transistor (Q1) increases to a predetermined rate to turn transistor (Q1) on. The predetermined maximum current flowing through transistor (Q1) depends on the predetermined maximum voltage applied to the gate of transistor (Q1).

Regarding claims 7 and 21, because the ramp signal is proportional to the AC current through the main inductor L1, the PWM will start with a minimum pulse width and increases until the output of the PWM is within regulation (col. 12, lines 13-36).

Regarding claims 8 and 9, the pulse width modulation switching regulator controller circuit (PWM) will start when the voltage applied to the pulse width modulation switching regulator controller circuit approaches the predetermined voltage of "the (active) source of power". Note that when the power supply applied to the circuit reaches a predetermined value, the pulse width modulation switching regulator controller circuit (PWM) will start.

Regarding claims 10 and 11, the active level of the output of the PWM is a high level. When the voltage applied to the (-) input of the PWM is lower (approaching) than the source voltage applied to the (+) input, the PWM start to activate circuit (902). When the voltage applied to the (-) input of the PWM is higher (approaching) than the source voltage applied to the (+) input, the PWM will not start to activate circuit (902).

Regarding claim 12, the switching transistors are transistors (Q2, Q3),

Regarding claim 15, figure 1 Patel shows a hot swappable pulse width modulation switching regulator controller comprising:

a hot swap transistor (Q1);

a converter output circuit (Q3, L1, R1-R3, ESR, Cout);

a pulse width modulator (PWM COMP);

a hot swap circuit (901) coupled to a control terminal of the hot swap transistor; the hot swap circuit for turning on the hot swap transistor at a controlled rate; whereby power is applied to the pulse width modulation controller at a controlled rate in spite switching regulator of the sudden application of power to the hot swappable pulse width modulation switching regulator controller (col. 12, lines13-48).

Regarding claims 16-19, because of the (PWM), control circuit (902) and the transformer (T2), the control voltage applied to the gate of transistor (Q1) increases to a predetermined rate to turn transistor (Q1) on. The predetermined maximum current flowing through transistor (Q1) depends on the predetermined maximum voltage applied to the gate of transistor (Q1). Hot swap transistor (Q1) is part of the integrated circuit.

Regarding claim 21, because the ramp signal is proportional to the AC current through the main inductor L1, the PWM will start with a minimum pulse width an increases until the output of the PWM is within regulation (col. 12, lines 13-36).

Regarding claims 22 and 23, the active level of the output of the PWM is a high level. When the voltage applied to the (-) input of the PWM is lower (approaching) than the source voltage applied to the (+) input, the PWM start to activate circuit (902). When the voltage applied to the (-) input of the PWM is higher (approaching) than the source voltage applied to the (+) input, the PWM will not start to activate circuit (902).

Regarding claims 24 and 25, the active level of the output of the PWM is a high level. When the voltage applied to the (-) input of the PWM is lower (approaching) than the source voltage applied to the (+) input, the PWM start to activate circuit (902). When the voltage applied to the (-) input of the PWM is higher (approaching) than the source voltage applied to the (+) input, the PWM will not start to activate circuit (902).

Regarding claim 28, figure 7 and 10 of Patel shows a method operating a switching converter having controller comprising:

a) when voltage is first supplied to the converter, increasing the voltage applied to the switching converter controller at a controlled rate (Q1 is turned on/of with a controlled rate);

b) when the voltage applied to the switching converter controller approaches the voltage supplied to the converter, starting the switching converter controller with a minimum pulse width (the ramp signal is proportional to the AC current through the main inductor L1 (col. 12 lines 26-29); and

c) increasing the pulse width until the converter comes into regulation. The ramp signal that creates the pulses is related to the output voltage thus, the pulse width increases until the converter comes into regulation (col. 12 lines 33-36).

Regarding claim 29, the active level of the output of the PWM is a high level. When the voltage applied to the (-) input of the PWM is lower (approaching) than the source voltage applied to the (+) input, the PWM start to activate circuit (902). When the voltage applied to the (-) input of the PWM is higher (approaching) than the source voltage applied to the (+) input, the PWM will not start to activate circuit (902).

Claims 15-18, 21, 22 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Boylan et al. US (Pat. 5,282,123).

Regarding claim 15, figure 1 of Boylan shows a hot swappable pulse width modulation switching regulator controller comprising:

a hot swap transistor (12);

a converter output circuit (20, 21, 23, 24, 25, 26);

a pulse width modulator (15);

a hot swap circuit (13) coupled to a control terminal of the hot swap transistor; the hot swap circuit for turning on the hot swap transistor at a controlled rate; whereby power is applied to the pulse width modulation controller at a controlled rate in spite switching regulator of the sudden application of power to the hot swappable pulse width modulation switching regulator controller (col. 2, lines26-44).

Regarding claims 16, 17 and 18, because of the PWM (15), hot swap circuit (13), circuits (31 and (14), the control voltage applied to the gate of transistor (12) increases to a predetermined rate to turn transistor (12) on. The predetermined maximum current flowing through transistor (12) depends on the predetermined maximum voltage applied to the gate of transistor (12).

Regarding claim 21, the pulse width starts with a small value and the PWM will start with a minimum pulse width and increases until the output of the PWM is within regulation.

Regarding claim 22, the active level of the output of the PWM is a high level for turning transistors (110 and (12) on when the voltage applied to the PWM start to rise.

Regarding claim 28, figure 1 of Boylan shows a method operating a switching converter having controller comprising:

a) when voltage (Vin) is first supplied to the converter, increasing the voltage applied to the switching converter controller at a controlled rate (transistor 12 is turned on/off with a controlled rate generated by the PWM 15);

b) when the voltage applied to the switching converter controller approaches the voltage supplied to the converter, starting the switching converter controller with a minimum pulse width. Note the output pulse of the PWM (15) varies with the input voltage (see USP. 5,282,123, col. 12, lines 13-36).

c) increasing the pulse width until the converter comes into regulation.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 6, 12, 13, 19, 20 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel et al. US (Pat. 6,456,510).

Regarding claims 5, 12, 13 and 19, figures 7 and 10 of Patel includes all the limitations of these claims except for the limitation that the components of the circuit (hot swap transistor and converter switching transistors) are on the integrated circuit. However, it is old and well known that with the new IC technique, all elements of a circuit can be fabricated on a piece of silicon (IC circuit) for reducing the size thus, minimizing the fabrication cost. Therefore, it would have been obvious to those skilled in the art to fabricate the circuit of Patel in integrated form for cutting cost and reducing size.

Regarding claims 6, 20 and 26 figure 7 of Patel includes all the limitations of these claims except for the limitation that the hot swap transistor is a discrete transistor. It is old and well known that a discrete transistor has a larger size than a transistor built on an IC circuit and a discrete transistor can conduct a large current. Therefore, it would have been obvious to those skilled in the art to replace the hot swap transistor (Q1) of Patel with a discrete transistor in case a large driving current is required.

Response to Arguments

In the Remarks, page 8, the Applicant argues that Q1 is not a "hot swap transistor" and "the pulse width modulation switching regulator controller circuit and the hot swap circuit inherently being in a single integrated circuit" is clearly incorrect". The invention, figure 2 of the present application is a pulse width modulation circuit comprising a transistor (Qhs) so called "hot swap transistor" controlled by a circuit (30) so called "hot swap circuit" for regulating the flow of current in the transformer (T1). Figure 10 of Patel is a pulse width modulation circuit comprising transistor (Q1) for regulating the flow of current in the transformer (T1). Thus, the circuit of Patel and the circuit of the present application are similar and transistor (Q1) can be labeled to be the hot swap transistor and circuit (901) can be labeled to be the hot swap circuit. The labels of the claimed components of a circuit do not make the claimed circuit distinguished from the prior art. The Applicant also argues that "Patel clearly does not show a single integrated circuit. Column 3, lines 40-43 and column 5 lines 15-20 disclose that the pulse width modulator of Patel is a part of an I/O circuit and the I/O circuit is built in an integrated circuit (ASIC).

In page 9, the Applicant argues that: "With respect to claim 7, it should be note that because the error signal is maximum at startup, a pulse width modulator will normally start with a maximum pulse width (?) and decrease until the output is within regulation. This argument is not true because comparator (PWMCOMP) of Patel compares a saw tooth signal with an error signal. When the error signal starts with a maximum value, the pulse with is minimum and the pulse width is larger when the error signal decreases.

In page 9 and 10, the Applicant argues that transistor 12 in Boyland is not a hot swap transistor, but rather a switching transistor as part of the pulse width modulator. As discussed above, the invention, figure 2 of the present application is a pulse width modulation circuit comprising a transistor (Qhs) so called "hot swap transistor" controlled by a circuit (30) so called "hot swap circuit" for regulating the flow of current in the transformer (T1). Figure 1 of Boylan is a pulse width modulation circuit comprising transistor (12) for regulating the flow of current in the transformer (17). Thus, the circuit of Boylan and the circuit of the present application are similar and transistor (12) is considered to be a hot swap transistor.

The Applicant also argues that fabricating the circuit of Patel in an IC for cutting cost and reducing size is a hindsight. It is well know that every electronic element including capacitors and inductors can be built in an IC for cutting cost and reducing size thus, the circuit of Patel also can be built on an IC for these above reasons. Moreover, column 3, lines 40-43 and column 5 lines 15-20 disclose that the pulse width modulator of Patel is a part of an I/O circuit and the I/O circuit is built in an integrated circuit (ASIC).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
02-18-06

TUAN T. LAM
PRIMARY EXAMINER